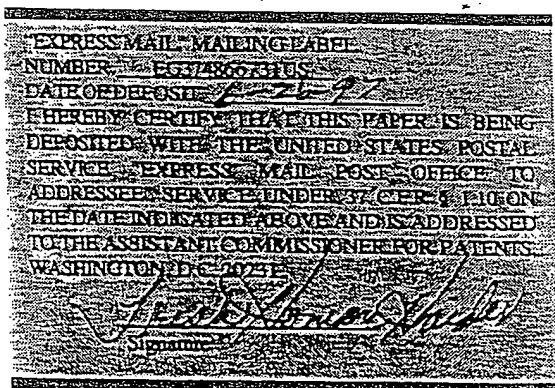APPLICATION FOR LETTERS PATENT

FOR

A CIRCUIT AND METHOD TO PREVENT
INADVERTENT TEST MODE ENTRY

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A CIRCUIT AND METHOD TO PREVENT
INADVERTENT TEST MODE ENTRY

Technical Field

This invention relates generally to integrated circuit devices and, more specifically, to a circuit and method for controlling the ability of such devices to enter into a test mode.

Background of the Invention

The testing of memory devices in the prior art generally involves receiving inputs from several memory addresses at one time into a test vector decoding circuit and performing logic functions on those inputs. The resulting output test vectors are used to perform operations on various devices, such as compressing address circuits or disabling regulators. Once testing has been completed, the values of the output test vectors will remain consistent for the purpose of driving circuits during non-test operations of the memory device.

One possible method of triggering the test mode as disclosed in the prior art is to use two signals. For example, a WCBR signal (Write enable signal at low with the CAS signal transmitted Before the RAS signal) sent during the transmission of a supervoltage signal is often used. The supervoltage signal will have a higher potential than the standard supply voltage. This supervoltage signal may generally be applied consistently throughout both test and non-test modes of the memory device. Only during the test mode, however, will the WCBR signal deliberately appear.

Nevertheless, it is possible that placing the memory device in a noisy environment may result in an errant WCBR signal being sent to the test vector decode circuit during a non-test mode. For example, memory devices are often subjected to a burn-in process, wherein the memory devices are operated at higher-than-usual voltages and temperatures in order to identify weak memory devices. This noisy process could result in random signals being transmitted through the write enable, CAS, and RAS paths so as to trigger a false WCBR signal and latch the test vector decode circuit. In that event, the test vector decode circuit would process the memory address inputs at their present random state. The resulting output vectors might not have the proper values. As a consequence, parts of the integrated device that should receive a particular value may no longer do so. For example, it is possible that one of the output vectors may represent an errant "ground V_{BB}" signal transmitted at the wrong time. That would ground the substrate of the memory device, thereby causing a high current mode and eventual meltdown of the circuitry. Therefore, it would be a benefit to the art to be able to prevent the memory circuit from inadvertently entering a test mode.

Summary of the Invention

Accordingly, one embodiment of the present invention provides a lockout circuit for an operations circuit. The operations circuit is configured to receive one or more sets of inputs. Upon receiving a latching signal, the operations circuit performs a decode operation on the present set of inputs A_0 through A_n. The decode operation, in turn, establishes a value for one or more output vectors in response to a latch signal. Further, a disable vector is included as one of the output vectors. At least one of the input sets is configured to establish a lockout value for the disable vector. Thus, once the appropriate set is input and latched, the resulting disable vector prevents inadvertent latching signals from reaching the operations circuit. However, the operations circuit is also configured to receive a reset signal and reset the disable vector in response to that signal.

In another embodiment, the operations circuit is a test vector decode circuit configured to receive a supervoltage signal. The supervoltage signal is generally maintained during all operations of the test vector decode circuit. The test vector decode circuit is configured to reset all output vectors in response to turning off the supervoltage

5   signal. In addition, the latching signal is combined with the disable vector through logic circuitry before reaching the test vector decode circuit. Latching operations proceed as described above until the disable vector changes the logic circuitry output, thereby locking out further latching signals. Once that occurs, the output vectors will not change unless the supervoltage signal is removed. In that event, all of the test vectors would be

10   reset and any errors in the operation of the memory circuit could more likely be traced to the interruption of the supervoltage signal rather than to inadvertent latching signals. Thus, in addition to the advantages of preventing inadvertent activation of the test mode using a minimal amount of die space, this embodiment also simplifies error detection and correction.

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Still other exemplary embodiments operate similarly but use different logic circuitry configurations. Further, the test vector decode circuits in these embodiments are configured to enable latching and resetting in a manner consistent with the logic circuitry configurations.

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Brief Description of the Drawings

Figure 1 depicts a schematic diagram of a test mode circuit as exists in the prior

25   art.

Figure 2 is a timing diagram illustrating the combined input signals used, both in the prior art and in an exemplary embodiment of the claimed invention, to latch the test vectors to output.

Figure 3 is a schematic diagram of one exemplary embodiment of the present invention.

Figure 4 is a schematic diagram of a second exemplary embodiment of the present
5   invention.

Figure 5 is a schematic diagram of a third exemplary embodiment of the present invention.

10   Figure 6 is a schematic diagram of a fourth exemplary embodiment of the present invention.

Figure 7 is a schematic diagram of a fifth exemplary embodiment of the present invention.

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Figure 8 is a schematic diagram of a sixth exemplary embodiment of the present invention.

20   <u>Detailed Description of the Preferred Embodiments</u>

As Figure 1 demonstrates, testing the operation of a memory circuit as taught by
the prior art is generally performed by directing signals to a test vector decode circuit 10
from a plurality of memory addresses A_0 through An, wherein n is an integer. The test
25   vector decode circuit 10 is usually a multiplexer, but regardless of the specific
configuration of the test vector decode circuit 10, it will subject the inputs to one or more
logic operations and generate a plurality of output test vectors V_0 through Vm, wherein m
is an integer that may or may not be equal to integer n. In addition, a supervoltage detect
circuit 12 is provided and is configured to respond to an external signal P by transmitting
30   a supervoltage signal (SV) to a reset input terminal 14 of the test vector decode circuit 10.

The test vector decode circuit 10 resets all output test vectors V_0 through Vm in response to a low SV signal. Thus, as long as SV remains at a high supervoltage potential, the output test vectors V_0 through Vm maintain the values established as of the last logic operation. Logic operations are initiated by a signal sent to a latch input terminal 16 of

5   the test vector decode circuit 10. In this embodiment, the test vector decode circuit 10 is configured to allow latching of the output test vectors V_0 through Vm in response to a low WCBR signal, designated in Figure 1 as WCBR*. This WCBR* signal is output by a WCBR detect circuit 18 which receives the signals RAS (Row Address Strobe), CAS (Column Address Strobe), and WE (Write Enable). Figure 2 demonstrates the required

10   state of these signals in order to latch the output test vectors: if (1) WE is low, and (2) CAS transmits a low signal before RAS does, then the WCBR circuit will output a WCBR* signal for latching the output test vectors V_0 through Vm. Figure 2 also illustrates the cycle length of the test vectors in relation to the duration of the three signals. After the output test vectors V_0 through Vm have been latched, they are used to

15   drive external devices. Further inputs and latchings may be used to alter the drive of these external devices. Once testing is over, however, the drive signals should generally maintain their value.

      The combination of signals generating WCBR is chosen to trigger the latching of

20   the output vectors because that combination is not intentionally used during non-test operations of the memory device. This reduces the chance of accidental latching and changing of the output test vectors at inappropriate times. As mentioned above, however, that combination of signals may appear as a glitch in noisy environments such as the burn-in process.

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      In order to prevent such accidental latching and the resulting consequences, a preferred embodiment of the present invention provides an additional output test vector V_{dis} that is used in conjunction with a logic unit such as an OR gate 20 to lock out further WCBR* signals. As shown in Figure 3, the OR gate 20 is electrically interposed between

30   the WCBR detect circuit 18 and the latch input terminal 16. As a result, the WCBR*

signal serves as a first input for the OR gate 20. The output test vector V_{dis} serves as a second input for the OR gate 20. Initially, V_{dis} transmits a low signal and WCBR* transmits a high signal. As a result, the OR gate 20 outputs a high signal and there is no latching.

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When CAS is transmitted before RAS with WE at low, the WCBR* signal changes to low. The OR gate 20 recognizes the change. Accordingly, the output of OR gate 20 also changes to low and allows electrical communication within the test vector decode circuit 10. As a result of the decode operations performed on the inputs, the
10   values of one or more output vectors are established. If V_{dis} is one of the output vectors affected by the inputs, then V_{dis} will generate and maintain a high signal. This signal, which can be described as a "lockout" signal for purposes of this application, changes the OR gate 20 output back to a high signal. Regardless of further changes in the WCBR* signal, the OR gate 20 will continue to output a high signal as long as V_{dis} is high. Thus,
15   the high signal from V_{dis} blocks any other output test vector from being latched, and the test mode is ended. The only way this test vector lockout mode can be changed is if a low SV signal is transmitted to the reset input terminal 14. Doing so activates the reset function of the test vector decode circuit 10. Therefore, if the tested devices are operating in an unexpected manner, it is more likely that such a problem would be due to the
20   supervoltage signal and its related circuitry rather than to accidental latching of the output test vectors.

Moreover, the current invention covers other embodiments having different lockout configurations. For example, Figure 4 illustrates that the OR gate can be replaced
25   by another logic unit, such as a NOR gate 22. While the required input values remain the same as in the previous embodiment, the test vector decode circuit 10 is now configured to allow latching in response to a high signal received at the latch input terminal 16. Thus, before lockout, V_{dis} transmits a low signal. Accordingly, the NOR gate 22 will transmit a high latch enable signal in response to the low WCBR* input. Once the
30   appropriate inputs are decoded to change the value of V_{dis} to a high signal, the NOR gate

22 will continue to transmit a low signal, regardless of further low WCBR* signals, until the output vectors are reset.

5   In addition to using other logic units, one could choose to enable a lockout mode in response to different inputs. In Figure 5, the test vector decode circuit 10 is once again configured to enable latching in response to a high signal. In this embodiment, however, the enabling signal comes from the output of an AND gate 24. Furthermore, V_{dis} is initially transmitting a high signal rather than a low one. Thus, latching will occur during this V_{dis} state when WCBR* is high rather than low. In order to lock out further WCBR*

10   signals, the V_{dis} vector must be changed to low by decoding the proper input values.

     Figure 6 depicts yet another embodiment, wherein the test vector decode circuit 10 is configured to allow latching in response to a low signal output from a NAND gate 26. As in the previous embodiment, a high WCBR* signal will cause latching only as

15   long as V_{dis} transmits a high signal.

     It should be further noted that WCBR* and SV are not the only signals that could be used to latch and reset the output vectors. They have been identified in this specification for demonstrative purposes only. Figure 7 illustrates that, in general, all that

20   is needed is some sort of operations circuit 28 configured to receive at least one input A, perform some function based on that input, and transmit at least one output B. In addition, the operations circuit 28 is configured to perform its function in response to receiving a function prompt signal 30. However, that signal 30 is subject to being blocked by any embodiment of the current invention, such as some form of lockout

25   circuit 32. Nevertheless, the operations circuit 28 could be configured to once again receive the latching prompt signal in response to a reset prompt signal 34.

     One of ordinary skill can appreciate that, although specific embodiments of this invention has been described for purposes of illustration, various modifications can be

30   made without departing from the spirit and scope of the invention. For example, the

memory device could be configured to provide a test vector lockout signal from an external device 22 that is independent from the test vector decode circuit 10 and the output test vectors V_0 through Vm, as shown in Figure 8. Furthermore, resetting the test vector lockout signal could also be independent from resetting all other output vectors.

5   Such an embodiment could comprise sending a reset signal directly to the external device 22. Accordingly, the invention is not limited except as stated in the claims.